WHAT IS CLAIMED IS:

1. A clock control circuit comprising

at least one timing averaging circuit which generates and outputs from an output terminal, a signal having a time difference obtained by internally dividing a time difference between first and second signals, which are input respectively from first and second input terminals, at a prescribed ratio,

wherein first and second clock signals are supplied respectively to the first and second input terminals of said timing averaging circuit, and a clock signal having a time difference obtained by internally dividing a time difference between pulses of the first and second signals is generated.

2. A clock control method for reducing jitter, comprising the steps of:

providing a timing averaging circuit which generates, and outputs from an output terminal, a signal having a time difference obtained by internally dividing a time difference between first and second signals, which are input respectively from first and second input terminals, at a prescribed ratio;

inputting first and second clock signals having a time difference between them to said timing averaging circuit; and

generating a clock signal having a time difference obtained by internally dividing a time difference between pulses of the first and second clock signals to reduce jitter.

3. A clock control circuit comprising:

a timing averaging circuit which includes at least one timing dividing circuit that generates, and outputs from an output terminal, a signal which undergoes a transition after a delay equivalent to a time difference obtained by internally dividing a time difference between first and second signals, which are input respectively to first and second input terminals, at a prescribed ratio, said delay being in response to rising and/or falling edge of the first and/or second signal; and

a stage of dividing an entered clock into first and second clock signals and applying the first and second clock signals to said timing averaging circuit.

4. A clock control circuit comprising:

(a) a plurality of serially connected timing averaging circuits each having two parallel-connected timing dividing circuits, said timing dividing circuits generating, and outputting from an output terminal, a signal which undergoes a transition after a delay equivalent to a time difference obtained by internally dividing a time difference between first and second signals, which are input respectively to first and second input terminals, wherein transition timing of the first or second signal, whichever is earlier, is used as a reference;

(b) wherein first and second clock signals are input respectively to first and second input terminals of each of said timing dividing circuits that constitute a first stage of said timing averaging circuits;

(c) wherein first and second output signals, which are output from the output terminals of each of said timing dividing circuits of a timing averaging circuit of a preceding stage, are input respectively to first and second input terminals of each of said timing dividing circuits that constitute a timing averaging circuit of a succeeding stage; and

(d) wherein first and second output signals from the output terminals of each of the timing dividing circuits of a timing averaging circuit of a final stage are extracted.

5. The clock control circuit according to claim 3, wherein timing averaging circuits each obtained by arranging said timing dividing circuits in parallel to support the number of phases of an input multiphase clock signal are serially connected in a plurality of stages.

6. The clock control circuit according to claim 4, wherein timing averaging circuits each obtained by arranging said timing dividing circuits in parallel to support the number of phases of an input multiphase clock signal are serially connected in a plurality of stages.

7. A clock control circuit comprising:

(a) a stage to which a plurality of clocks of mutually different phases are input, this stage generating a plurality of control signals corresponding to transition timing of one clock of the plurality of clocks and to phase differences between the clocks;

(b) a switch group, whose switching is controlled by the control

signals, of controlling charging and discharging of a capacitor;

(c) a stage of converting terminal voltage of the capacitor to a logic signal and outputting the logic signal;

(d) a stage of varying charging or discharging speed of the capacitor by shifting switching control timings of switches in said switch group; and

(e) a timing dividing circuit that outputs a clock signal having a phase difference obtained by internally dividing the phase difference between the clocks.

8. A clock control circuit comprising:

(a) at least one timing dividing circuit that generates a signal having a phase difference obtained by internally dividing a phase difference between a predetermined set of clock phases of multiphase clocks having mutually different phases, said timing dividing circuit being provided in a number equivalent to the number of clock phases;

(b) a stage of generating a signal having a duration equivalent to the phase difference between a predetermined pair of outputs regarding outputs of the plurality of timing dividing circuits; and

(c) a stage of generating a multiphase clock by combining two signals of a predetermined pair regarding these signals generated in a number equivalent to the number of clock phases.

9. A clock control circuit comprising:

(a) a plurality of serially connected timing averaging circuits

each having two parallel-connected timing dividing circuits that generate, and output from an output terminal, a signal which undergoes a transition after a delay equivalent to a time difference obtained by internally dividing a time difference between first and second signals, which are input respectively to first and second input terminals, wherein transition timing of the first or second signal, whichever is earlier, is used as a reference;

(b) frequency divider circuit that frequency divides an entered clock signal to first and second clock signals and outputting the first and second clock signals;

(c) wherein the first and second clock signals from said frequency divider circuit are input respectively to first and second input terminals of each of said parallel-connected timing dividing circuits that constitute a first stage of said timing averaging circuits;

(d) wherein first and second output signals, which are output from the output terminals of each of said timing dividing circuits of a timing averaging circuit of a preceding stage, are input respectively to first and second input terminals of each of said timing dividing circuits that constitute a timing averaging circuit of a succeeding stage; and

(e) a combining circuit, to which first and second output signals from the output terminals of each of the timing dividing circuits of a timing averaging circuit of a final stage are input, said

combining circuit outputting these signals upon multiplexing the same.

10. The clock control circuit according to claim 3 , wherein said timing dividing circuits each have:

(a) first and second switch elements which switch in response to transition of the first and second input signals,

(a1) wherein one of the switch elements is turned ON in response to transition of one of the first and second input signals, to cause current to flow through the ON switch element to charge a capacitor, and

(a2) wherein both switch elements then being turned ON in response to transition of the second signal, to change the capacitor at a varied charging speed; and

(b) a stage of outputting terminal voltage of the capacitor as a logic signal;

(b1) wherein there is generated an output signal which undergoes a transition at a time difference obtained by internally dividing a time difference between the first and second input signals at a prescribed ratio, transition time of the first or second input signal serving as a reference for the time difference.

11. The clock control circuit according to claim 4, wherein a ratio at which the time difference is internally divided is variable.

12. The clock control circuit according to claim 3, wherein said

timing dividing circuits each have:

(a) at least first and second switch element groups each including first and second switch elements each turned ON and OFF, respectively, by rising and falling edges of the first and second input signals,

(b) switching sequence of the switch elements of the first group being controlled in dependence upon one of a rising edge and falling edge of the first and second input signals,

(c) wherein charging speed of the capacitor is varied during a process of charging the capacitor, switching sequence of the switch elements of the second group being controlled in dependence upon the other one of the rising edge and falling edge of the first and second input signals, whereby discharging speed of the capacitor is varied during a process of charging the capacitor; and

(d) a stage of outputting terminal voltage of the capacitor as a logic signal;

(e) wherein there is generated a signal which undergoes a transition at a time difference obtained by internally dividing a time difference between the first and second input signals, the first or second input signal serving as a reference for the time difference.

13. A timing averaging circuit comprising:

parallel-connected timing dividing circuits that generate, and output from an output terminal, a signal having

a time difference obtained by internally dividing a time difference between first and second signals, which are input respectively to first and second input terminals, wherein transition timing of the first or second signal, whichever is earlier, is used as a reference.

14. A timing dividing circuit comprising:

(a) first and second switch elements turned ON and OFF in response to transitions of first and second input signals input respectively from first and second input terminals,

(a1) wherein one of the switch elements is turned ON in response to transition of one of the first and second input signals, whereby current flows through the ON switch element to charge a capacitor, and

(a2) wherein both switch elements then are turned ON in response to transition of the second signal, whereby charging speed of the capacitor is varied; and

(b) a stage of outputting terminal voltage of the capacitor as a logic signal;

(c) wherein there is generated an output signal which undergoes a transition at a time difference obtained by internally dividing a time difference between the first and second input signals, transition time of the first or second input signal serving as a reference for the time difference.

15. A timing dividing circuit comprising:

(a) at least first and second switch element groups that include

first and second switch elements each turned ON and OFF by rising and falling edges of first and second input signals input respectively from first and second input terminals,

(b)a stage of controlling switching sequence of the switch elements of the first group in dependence upon one of a rising edge and falling edge of the first and second input signals, to vary charging speed of the capacitor during a process of charging the capacitor,

(c) a stage of controlling switching sequence of the switch elements of the second group in dependence upon the other one of the rising edge and falling edge of the first and second input signals, to vary discharging speed of the capacitor during a process of charging the capacitor; and

(d) a stage of outputting terminal voltage of the capacitor as a logic signal;

(e) wherein there is generated a signal which undergoes a transition at a time difference obtained by internally dividing a time difference between the first and second input signals, the first or second input signal serving as a reference for the time difference.

16. The timing dividing circuit according to claim 15, wherein said first and second switch element groups are each constructed using transistors of NAND and NOR gates as basic gates.

17. A clock control circuit comprising:

(a) a fixed delay circuit that delays an input signal by a

predetermined phase; and

(b) a timing averaging circuit that generates, and outputs from an output terminal, a signal having a time difference obtained by internally dividing a time difference between first and second signals input respectively from first and second input terminals;

(c) wherein an entered clock signal is applied to said fixed delay circuit chain, the entered clock signal and an output of said fixed delay circuit chain are applied to said timing averaging circuit, and a clock is extracted from the output terminal of said timing averaging circuit.

18. The clock control circuit according to claim 17, wherein said fixed delay circuit chains delays the entered signal by 360 degrees that is one cycle.

19. The clock control circuit according to claim 17, wherein said fixed delay circuit chain comprises two serially connected stages of fixed delay circuit chains each of which delays the entered signal by 180 degrees that is a half cycle.

20. The clock control circuit according to claim 16, wherein said fixed delay circuit chain comprises a synchronous delay circuit chain which includes:

(a) a first delay circuit along a fixed length of which an input pulse is caused to travel;

(b) a second delay circuit chain through which a pulse is caused to travel along a length equal or proportional to the length

along which the pulse traveled through said first delay circuit chain; and

(c) a control circuit that controls transfer of a pulse from the first delay circuit chain to the second delay circuit chain.

21. A clock control circuit of a semiconductor integratesd circuit device for generating an internal clock from an entered external clock, comprising:

(a) a delay-locked loop adapted to vary delay of the input signal, and having at least a phase-difference sensing circuit, a charge pump, a loop filter and a voltage-controlled delay circuit, to which an output from said loop filter is input as a control voltage;

(b) a timing averaging circuit generating a signal having a time difference obtained by internally dividing, at a prescribed ratio, a time difference between two signals that are input with a fixed time difference between them;

(c) wherein an output of said voltage-controlled delay circuit is supplied as an internal clock via a clock driver; and

(d) wherein a clock signal, which is input to said phase-difference sensing circuit, obtained by inputting the external clock via an input buffer, and a signal obtained by passing said internal clock through an input buffer dummy circuit having a delay time equivalent to that of said input buffer are applied to said timing averaging circuit, with an output of said timing averaging circuit being applied as an input signal to said

voltage-controlled delay circuit.

22. The clock control circuit according to claim 21, wherein in said timing averaging circuit, internal-division ratio is decided in such a manner that timing ratio of the internal clock signal is enlarged as the ratio at which the time difference is internally divided, to said timing averaging circuit being input the external clock from said input buffer and the internal clock signal supplied from said voltage-controlled delay circuit through said clock driver and said input buffer dummy circuit.

23. The clock control circuit according to claim 21, further comprising:

(e) a lock sensing circuit for sensing a locked state from the output of said phase-difference sensing circuit; and

(f) a changeover circuit supplying said phase-difference sensing circuit with either the input clock or the output of said timing averaging circuit;

(g) wherein after locking is sensed, said changeover circuit changes over the signal supplied to said phase-difference sensing circuit from the external clock input from said input buffer to a signal obtained by internally dividing the time difference between the external clock and the input clock by said timing averaging circuit.

24. A delay-locked loop circuit comprising:

(a) at least a phase-difference sensing circuit, a charge pump, a loop filter and a voltage-controlled delay circuit, to which

an output from said loop filter is input as a control voltage, to vary delay of the input signal; and

(b) a timing averaging circuit generating a signal having a time difference obtained by internally dividing, at a prescribed ratio, a time difference between two signals that are input with a fixed time difference between them;

(c) wherein said timing averaging circuit is supplied with an input clock signal entering said phase-difference sensing circuit and an output signal from said voltage-controlled delay circuit, an output of said timing averaging circuit being applied as an input signal to said voltage-controlled delay circuit.

25. The delay-locked loop circuit according to claim 24, further comprising:

(d) a lock sensing circuit sensing a locked state from the output of said phase-difference sensing circuit; and

(e) a changeover circuit supplying said phase-difference sensing circuit with either the input clock or the output of said timing averaging circuit;

(f) wherein after locking is sensed, said changeover circuit changes over the signal supplied to said phase-difference sensing circuit from the input clock to a signal derived from said timing averaging circuit.

26. A clock control circuit of a semiconductor integrated circuit device for generating an internal clock from an entered

external clock, comprising:

(a) a phase synchronizing loop circuit having at least a phase-difference sensing circuit, a charge pump, a loop filter and a voltage-controlled oscillator circuit;

(b) a timing averaging circuit generating a signal having a time difference obtained by internally dividing, at a prescribed ratio, a time difference between two signals that are input with a fixed time difference between them;

(c) wherein said timing averaging circuit is supplied with a clock signal, which is obtained by inputting the external clock via an input buffer, and a signal obtained by passing an internal clock, which is obtained by outputting a signal from said voltage-controlled oscillator via a clock driver, through an input buffer dummy circuit having a delay time equivalent to that of said input buffer;

(d) a lock sensing circuit sensing a locked state from the output of said phase-difference sensing circuit; and

(e) a changeover circuit supplying said phase-difference sensing circuit with either the input clock or the output of said timing averaging circuit;

(f) wherein after locking is sensed, said changeover circuit changes over the signal supplied to said phase-difference sensing circuit from the input clock to a signal output from said timing averaging circuit.

27. A phase synchronizing loop circuit having at least a

phase-difference sensing circuit, a charge pump, a loop filter and a voltage-controlled oscillator circuit, comprising:

(a) a timing averaging circuit generating a signal having a time difference obtained by internally dividing, at a prescribed ratio, a time difference between two signals that are input with a fixed time difference between them;

(b) wherein said timing averaging circuit is supplied with an input clock signal and an output signal from said voltage-controlled oscillator circuit, and an output of said timing averaging circuit is applied as one input of said phase-difference sensing circuit.

28. The phase synchronizing loop circuit according to claim 27, further comprising:

(c) a lock sensing circuit sensing a locked state from the output of said phase-difference sensing circuit; and

(d) a changeover circuit supplying said phase-difference sensing circuit with either the input clock or the output of said timing averaging circuit;

(e) wherein after locking is sensed, said changeover circuit changes over the signal supplied to said phase-difference sensing circuit from the input clock to a signal output from said timing averaging circuit.

29. A clock control circuit of a semiconductor integrated circuit device to which an external clock is input for generating an internal clock, comprising:

(a) a synchronous delay circuit which includes:

(b) a first delay circuit chain through which a pulse or pulse edge is caused to travel for a fixed period of time;

(c) a second delay circuit chain capable of passing a pulse or pulse edge along a length thereof equal or proportional to the length along which the pulse or pulse edge traveled through said first delay circuit chain;

(d) a clock driver outputting an internal clock from an output of said second delay circuit chain; and

(e) a timing averaging circuit, to which are input a clock signal from an input buffer and a signal obtained by passing an internal clock signal, which is output via said clock driver, through an input buffer dummy circuit having a delay time equivalent to that of said input buffer, to generate and output a signal having a time difference obtained by internally dividing, at a prescribed ratio, a time difference between these two signals;

(f) wherein said first delay circuit chain is supplied with the output of said timing averaging circuit via a dummy delay circuit.

30. A clock control circuit of a semiconductor integrated circuit device to which an external clock is input for generating an internal clock, comprising:

(a) a synchronous delay circuit which includes:

(b) a first delay circuit chain through which a pulse or pulse edge is caused to travel for a fixed period of time;

(c) a second delay circuit chain capable of passing a pulse or pulse edge along a length thereof equal or proportional to the length along which the pulse or pulse edge traveled through said first delay circuit chain;

(d) a clock driver outputting an internal clock from an output of said second delay circuit; and

(e) first and second timing averaging circuits, to which are input a clock signal from an input buffer and a signal obtained by passing an internal clock signal, which is output via said clock driver, through an input buffer dummy circuit having a delay time equivalent to that of said input buffer, to generate and output a signal having a time difference obtained by internally dividing, at a prescribed ratio, a time difference between these two signals, said first delay circuit chain being supplied with the output of said first timing averaging circuit via a dummy delay circuit;

(f) wherein said first delay circuit chain is supplied with the output of said timing averaging circuit via a dummy delay circuit, and

(g) wherein the output of said second timing averaging circuit is supplied as a control signal for controlling transfer of a signal from said first delay circuit chain to said second delay circuit chain.

31. A clock control circuit of a semiconductor integrated circuit device to which an external clock is input for generating

an internal clock, comprising:

(a) a synchronous delay circuit which includes:

(b) two sets of delay circuit chains each of which includes:

(b1) a first delay circuit chain through which a pulse or pulse edge is caused to travel for a fixed period of time, and

(b2) a second delay circuit chain capable of passing a pulse or pulse edge along a length thereof equal or proportional to the length along which the pulse or pulse edge traveled through said first delay circuit; and

(c) first and second timing averaging circuits, to which are input a clock signal from an input buffer and a signal obtained by passing an internal clock signal, which is output via said clock driver, through an input buffer dummy circuit having a delay time equivalent to that of said input buffer, to generate and output a signal having a time difference obtained by internally dividing, at a prescribed ratio, a time difference between these two signals, said first delay circuit chain being supplied with the output of said first timing averaging circuit via a dummy delay circuit;

(d) wherein said first delay circuit chain of each set is supplied with the output of said first timing averaging circuit via a dummy delay circuit,

(e) wherein a frequency-divided signal obtained by frequency dividing the output of said second timing averaging circuit by a frequency divider circuit is supplied as a control signal for

controlling transfer of a signal from said first delay circuit chain of each set to said second delay circuit, and

(f) wherein an output from a changeover stage of alternately changing over between outputs of said second delay circuits of each of the sets is supplied to a clock driver and output from said clock driver as an internal clock.

32. The control circuit according to claim 29, wherein said dummy delay circuit comprises an input buffer dummy and a clock driver dummy circuit.

33. The control circuit according to claim 30, wherein said dummy delay circuit comprises an input buffer dummy and a clock driver dummy circuit.

34. The control circuit according to claim 31, wherein said dummy delay circuit comprises an input buffer dummy and a clock driver dummy circuit.

35. A clock control circuit of a semiconductor integrated circuit device to which an external clock is input for generating an internal clock, comprising

(a) a synchronous delay circuit chain which includes:

(b) a first delay circuit chain through which a pulse or pulse edge is caused to travel for a fixed period of time;

(c) a second delay circuit chain capable of passing a pulse or pulse edge along a length thereof equal or proportional to the length along which the pulse or pulse edge traveled through said first delay circuit chain;

(d) a monitor signal generating circuit for outputting a monitor signal for a period of time over which a clock pulse travels through an input buffer dummy circuit, which is equivalent to an input buffer to which the external clock is input, and a clock driver; and

(e) a timing averaging circuit, to which are input a clock signal from said input buffer and a signal obtained by passing an internal clock signal, which is output via said clock driver, through said input buffer dummy circuit, to generate a signal having a time difference obtained by internally dividing a time difference between these two signals, and outputting this signal to said first delay circuit chain;

(f) wherein travel of said pulse or pulse edge is halted in said first delay circuit chain while the monitor signal is being output.

36. The clock control circuit according to claim 35, further comprising:

(g) a first changeover circuit chain selecting one of a clock from said input buffer and an output of said timing averaging circuit and supplying it to said first delay circuit chain; and

(h) a second changeover circuit selecting and outputting one of a output of said first changeover circuit and an output of said second delay circuit chain.

37. The clock control circuit according to claim 36, wherein the output of said first changeover circuit and a signal input to

said timing averaging circuit via said clock driver and said input buffer dummy circuit are supplied to said monitor signal generating circuit.

38. A clock control circuit of a semiconductor integrated circuit device to which an external clock is input for generating an internal clock, comprising:

(a) a synchronous delay circuit which includes:

(b) a first delay circuit chain through which a pulse or pulse edge is caused to travel for a fixed period of time;

(c) a second delay circuit chain, to which a signal from said first delay circuit chain is input, capable of passing a pulse or pulse edge along a length thereof proportional to the length along which the pulse or pulse edge traveled through said first delay circuit chain;

(d) a monitor signal generating circuit outputting a monitor signal for a period of time over which a clock pulse travels through an input buffer dummy, which is equivalent to an input buffer, and a clock driver;

(e) first and second timing averaging circuits, to which are input a clock signal from said input buffer and an output from said input buffer dummy obtained by passage therethrough of an internal clock signal output via the clock driver, for generating a signal having a time difference obtained by internally dividing a time difference between these signals, and outputting this signal to said first delay circuit chain;

(f) wherein said first delay circuit chain of each set is supplied with the output of said first timing averaging circuit,

(g) wherein the output of said second timing averaging circuit is used as a signal for controlling transfer of a clock signal from said first delay circuit chain to said second delay circuit chain, and

(h) wherein travel of said pulse or pulse edge is halted in said first delay circuit chain while the monitor signal is being output; and

(i) a changeover circuit changing over between the output of said second delay circuit and the output of said input buffer, to supply the output to said clock driver.

39. A clock control circuit of a semiconductor integrated circuit device to which an external clock is input for generating an internal clock, comprising:

(a) a synchronous delay circuit which includes:

(b) two sets of delay circuits each of which includes:

(b1) a first delay circuit chain through which a pulse or pulse edge is caused to travel for a fixed period of time, and

(b2) a second delay circuit chain, to which a signal from said first delay circuit chain is input, capable of passing a pulse or pulse edge along a length thereof proportional to the length along which the pulse or pulse edge traveled through said first delay circuit chain;

(c) first and second timing averaging circuits, to which are

input a clock signal from an input buffer and a signal obtained by passing an internal clock signal, which is output via said clock driver, through an input buffer dummy circuit having a delay time equivalent to that of said input buffer, to generate and output a signal having a time difference obtained by internally dividing, at a prescribed ratio, a time difference between these two signals, said first delay circuit being supplied with the output of said first timing averaging circuit via a dummy delay circuit;

(d) a frequency divider circuit frequency dividing outputs from said first and second timing averaging circuits;

(e) wherein signals obtained by frequency dividing the outputs of said first and second timing averaging circuits by said frequency divider circuit are used as signals for controlling transfer of a clock signal from the first delay circuit chain of each set to said second delay circuit chain;

(f) a first changeover circuit alternately changing over between outputs of said second delay circuits of each of the sets every clock cycle; and

(g) a second changeover circuit for selecting the output of said input buffer or the output of said first changeover circuit, to supply the output to said clock driver.

40. A clock control circuit of a semiconductor integrated circuit device to which an external clock is input for generating an internal clock, comprising:

(a) a synchronous delay circuit which includes:

(b) a first delay circuit chain through which a pulse or pulse edge is caused to travel for a fixed period of time;

(c) a second delay circuit chain, to which a signal from said first delay circuit chain is input, capable of passing a pulse or pulse edge along a length thereof equal or proportional to the length along which the pulse or pulse edge traveled through said first delay circuit chain;

(d) a monitor signal generating circuit outputting a monitor signal for a period of time over which a clock pulse travels through an input buffer dummy, which is equivalent to an input buffer, and a clock driver;

(e) first and second timing averaging circuits, to which are input a clock signal from said input buffer and a signal obtained by passing an internal clock signal, which is output via the clock driver, through said input buffer dummy circuit, to generate a signal having a time difference obtained by internally dividing, at a prescribed ratio, a time difference between these two signals, and to output this signal to said first delay circuit chain;

(f) a first changeover circuit selecting the output of said input buffer or the output of said first timing averaging circuit, to supply the output to said first delay circuit chain; and

(g) a second changeover circuit changing-over between the output of said first changeover circuit and the output of said second

delay circuit chain;

(h) wherein the output of said second timing averaging circuit and the output of said second changeover circuit are connected to said monitor signal generating circuit, and travel of said pulse or pulse edge is halted in said first delay circuit while the monitor signal is being output.

41. A clock control circuit of a semiconductor integrated circuit device to which an external clock is input for generating an internal clock, comprising:

(a) a synchronous delay circuit which includes:

(b) a first delay circuit chain through which a pulse or pulse edge is caused to travel for a fixed period of time;

(c) a second delay circuit chain, to which a signal from said first delay circuit chain is input, capable of passing a pulse or pulse edge along a length thereof equal or proportional to the length along which the pulse or pulse edge traveled through said first delay circuit chain;

(d) a monitor signal generating circuit outputting a monitor signal for a period of time over which a clock pulse travels through an input buffer dummy, which is equivalent to an input buffer, and a clock driver;

(e) first, second and third timing averaging circuits, to which are input a clock signal from said input buffer and a signal obtained by passing an internal clock signal, which is output via the clock driver, through said input buffer dummy circuit,

to output a signal having a time difference obtained by internally dividing a time difference between these two signals;

(f) wherein the output of said first timing averaging circuit is input to said first delay circuit chain;

(g) wherein the output of said second timing averaging circuit is used as a signal for controlling transfer of a clock signal from said first delay circuit chain to said second delay circuit chain; and

(h) wherein the output of said third timing averaging circuit is connected to said monitor signal generating circuit; and

(i) a changeover circuit changing-over between the output of said second delay circuit and the output of said input buffer;

(j) wherein travel of said pulse or pulse edge is halted in said first delay circuit chain while the monitor signal is being output.

42. The clock control circuit according to claim 29, wherein delay circuit chain elements constructing said first delay circuit chain are clocked inverters controlled by said monitor signal.

43. The clock control circuit according to claim 35, wherein delay circuit chain elements constructing said first delay circuit chain are clocked inverters controlled by said monitor signal.

44. The clock control circuit according to claim 38, wherein delay circuit chain elements constructing said first delay

circuit are clocked inverters controlled by said monitor signal.

45. The clock control circuit according to claim 41, wherein delay circuit chain elements constructing said first delay circuit chain are clocked inverters controlled by said monitor signal.

46. The clock control circuit according to claim 29, wherein a signal input to each of said delay circuit chains is alternately driven by PMOS and NMOS transistors, first by PMOS transistors, then by NMOS transistors, every stage of said delay circuit chain.

47. The clock control circuit according to claim 29, wherein at the moment a signal input to said first delay circuit chain has traveled through said first delay circuit chain along a prescribed length thereof, the signal is transferred to said second delay circuit chain from a position thereof that corresponds to the prescribed length of said first delay circuit chain and then travels through said second delay circuit chain.

48. A clock control circuit of a semiconductor integrated circuit device to which an external clock is input for generating an internal clock, comprising:

(a) a synchronous delay circuit which includes:

(b) two sets of delay circuit chains each of which includes:

(b1) a first delay circuit chain through which a pulse or pulse edge is caused to travel for a fixed period of time, and

(b2) a second delay circuit chains capable of passing a pulse

or pulse edge along a length thereof equal or proportional to the length along which the pulse or pulse edge traveled through said first delay circuit chain;

(c) the delay circuit chains of each of the sets including a timing averaging circuit, to which two inputs are applied, internally dividing, at a prescribed ratio, a time difference between these two input signals;

(d) a monitor signal generating circuit for outputting a monitor signal for a period of time over which a clock pulse travels through an input buffer dummy, which is equivalent to an input buffer, and a clock driver;

(e) the output of said input buffer being input to a frequency divider circuit;

(f) the output of said input buffer being delivered as an internal clock via a first changeover circuit and being input to a second frequency divider and said monitor signal generating circuit via said input buffer dummy;

(g) the frequency-divided output of said frequency divider circuit being supplied to said first delay circuit chain of each of the sets and being supplied as a signal for controlling transfer from said first delay circuit chain of each set to said second delay circuit chain; and

(h) a second changeover circuit changing-over between outputs from the second delay circuit chains of each set;

(i) wherein the output of said changeover circuit and the output

of said input buffer are supplied to said first changeover circuit.

49. The clock control circuit according to claim 48, wherein control is performed in such a manner that after the monitor signal is output a first time, the next monitor signal is stopped.

50. The clock control circuit according to claim 48, wherein the delay circuit chains of each set each include a plurality of timing averaging circuits, and internal-division ratios of said timing averaging circuits are set independently of one another.

51. The clock control circuit according to claim 48, wherein said first and second delay circuit chains have first and second clocked inverters, which are arranged in parallel with respect to input signals, as a delay circuit of one stage, a common output node of said first and second clocked inverters is connected to the next stage, and

wherein a node of a stage having said first delay circuit chain is connected to a corresponding node of a stage having said second delay circuit chain.

52. The clock control circuit according to claim 48,

(j) wherein said first delay circuit chain through which a signal is caused to travel for a fixed period of time has first and second PMOS switches, provided in a delay circuit of one stage, turned ON by falling edges of first and second input signals, provided that turning ON of said first and second PMOS switches

in response to the falling edges of the first and second input signals, causes a common output node of said first and second PMOS switches to be charged from a power supply side;

(k) wherein said common output node is input to first and second NMOS switches of the next stage, said first and second NMOS switches of the next stage are turned ON in response to a rising edge of said common output node, whereby this output node is discharged to ground;

(l) said second delay circuit chain through which a signal propagates in a direction opposite that through which a signal travels through said first delay circuit chain has a PMOS switch and an NMOS switch provided in a stage corresponding to a PMOS switch and NMOS switch of each stage of said first delay circuit chain; and

(m) an output node of a PMOS switch stage of said first delay circuit chain is connected to an output node of an NMOS switch of a preceding stage of a PMOS switch corresponding to said stage in said second delay circuit chain.

53. A clock control circuit according to claim 50, wherein a path between the PMOS switch of each stage and the power supply and a path from an output load to ground via an NMOS switch are provided with switches turned ON and OFF, respectively, by the monitor signal.

54. A synchronous delay circuit wherein an input clock signal is alternately driven by a PMOS transistor and an NMOS transistor

in a delay circuit element constructing a delay circuit chain.

55. A synchronous delay circuit comprising:

(a) a first delay circuit chain through which a pulse or pulse edge is caused to travel for a fixed period of time; and

(b) a second delay circuit chain for passing a pulse or pulse edge along a length thereof equal or proportional to the length along which the pulse or pulse edge traveled through said first delay circuit chain, said pulse or pulse edge being passed through said second delay circuit chain from a stage corresponding to a position traveled by a signal through said first delay circuit chain;

(c) wherein said first and second delay circuit chains have a timing averaging circuit outputting a signal having a time difference obtained by internally dividing a time difference between two input signals.

56. The synchronous delay circuit according to claim 55, wherein the delay circuit chain of each stage includes a plurality of timing averaging circuits, an internal-division ratio of each timing averaging circuit being set independently.

57. The synchronous delay circuit according to claim 55, wherein delay circuit chains that include timing averaging circuits, each of which outputs a signal having a time difference obtained by internally dividing a time difference between two input signals, are serially connected.

58. The synchronous delay circuit according to claim 55, wherein

said first and second delay circuit chains have first and second clocked inverters, which are arranged in parallel with respect to an input signal, as a delay circuit of one stage, a common output node of said first and second clocked inverters is connected to the next stage, and

wherein a node of a stage having said first delay circuit chain is connected to a corresponding node of a stage having said second delay circuit chain.

59. A synchronous delay circuit

(a) wherein a first delay circuit chain through which a signal is caused to travel for a fixed period of time has first and second switch elements serving as charging switches, provided in a delay circuit chain of one stage, turned ON by falling edges of first and second input signals, and said first and second switch elements are turned ON successively in response to the rising edges of the first and second input signals, whereby a common output node of said first and second switch elements is charged from a power supply side;

(b) wherein said common connection mode is input to first and second switch elements, serving as discharging switches, of the next stage, said first and second switch elements of the next stage being turned ON in response to a rising edge of said common connection mode, whereby this output node is discharged to ground;

(c) wherein a second delay circuit chain through which a signal

propagates in a direction opposite that through which a signal travels through said first delay circuit chain has a charging switch and a discharging switch corresponding to each stage of the charging switch and discharging switch of said first delay circuit chain; and

(d) wherein an output node of the charging switch of each stage of said first delay circuit chain is connected to an output node of the discharging switch of a preceding stage of a charging switch corresponding to said stage in said second delay circuit chain.